Measurement of Dynamic Load Lines of Power Heterojunction Bipolar Transistor

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Abstract

Dynamic load lines of InGaP/GaAs Heterojunction Bipolar Transistors (HBTs) were experimentally measured with a load circuit tuned to maximum collector efficiency (η_C) and maximum gain. The phase relationship between the collector voltage and the collector current depended on the load circuit. The trajectory of the dynamic load line has a non-oval shape for the output power where gain compression heavily occurs.

Introduction

Although we have several device models for transistors, they do not explain very well how real transistors operate in high power regions due to, for example, the thermal effect. An experimental observation of a real output signal from a power transistor is very important to grasp the actual behavior of power amplifiers and to improve device models. Measurement of the dynamic load line is supposed to clarify, for example, the effects of harmonics on power amplifier performance. We focused the dynamic load lines of HBTs under gain-matched and η_C-matched operations. In this paper, we describe the dynamic load line measurement of HBTs as a beginning in understanding the operation of power HBTs.

Experiment

Fig. 1 shows a schematic of setup for the dynamic load line measurement. A packaged HBT was connected at port 1 to a pre-matching circuit followed by a bias-T. A coupler was connected between the bias-T and a load tuner. Port 3 and port 4 were connected to a transient analyzer to measure the magnitude and phase of the harmonics. From the reflected waves at port 3 and port 4 (b_3 and b_4 respectively), which were measured by the transient analyzer, the incident and reflected waves at port 1 (a_1, b_1) were calculated with the measured S-parameters between port 1, 2, 3 and 4 (S_{11}, S_{12}, ..., S_{44}). In this calculating, a_3 and a_4 are considered to be zero because the inputs to the transient analyzer are assumed to be perfectly matched. The following equations are to be solved for a_1 and b_1:

$$b_1=S_{11}a_1+S_{12}a_2$$
$$b_2=S_{21}a_1+S_{22}a_2$$
$$b_3=S_{31}a_1+S_{32}a_2$$
$$b_4=S_{41}a_1+S_{42}a_2$$

a_1 and b_1 are determined as follows:

$$a_1 = \frac{S_{42}b_3 - S_{32}b_4}{S_{31}S_{42} - S_{32}S_{41}}$$

$$b_1 = \frac{\left(S_{11}S_{42} - S_{12}S_{41}\right)b_3 + \left(S_{12}S_{31} - S_{11}S_{32}\right)b_4}{S_{31}S_{42} - S_{32}S_{41}}$$

The collector current and voltage are easily calculated by a_1 and b_1 [1].

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Loads for maximum gain and maximum η_c when P_{out} is 30.5 dBm were found by load pull measurement. Because a load line itself provides no information regarding the gain and input power level of the device, we prefer using the collector efficiency (η_c) over the power added efficiency (PAE) for the purpose of this experiment, which is to measure how the dynamic load line changes with the load state. The base and collector of the common-emitter HBT is quiescently biased with V_{be}=1.35 V and V_{ce}=3.5 V respectively, which results in I_c=210 mA. The HBT has an emitter configuration of 2 μm x 20 μm x 48 fingers[2]. The operation of the HBT is class AB. Fundamental frequency is 1.5 GHz. Incident power, reflected power and S-parameters were measured through the eighth harmonics.

Result and discussion

Fig. 2 shows the measured instantaneous collector current, i_c, and instantaneous collector voltage, v_c, when the load is tuned to maximum gain (case “G”). Fig. 3 shows the measured i_c and v_c when the load is tuned to maximum η_c (case “E”). Fig. 2 and Fig. 3 show the waveforms when P_{out} is about 30.5, 27.0 and 24.0 dBm. Table 1 summarizes the data measured in both cases. Reflection coefficient of harmonics calculated from a_1 and b_1 is shown in Table 2.

Let us compare the i_c and v_c waveforms of both cases when P_{out} is 30.5 dBm. In case “E”, the waveform of v_c is more square-like than in case “G”, and i_c reaches a maximum when v_c reaches its nadir, which is reasonable for a high-efficient transistor operation. As shown in Table 1, when P_{out} is 30.5 dBm, gain compression is much larger in case “E” than in case “G”. Gain compression is presumed to create harmonics and cause waveforms to diverge from a sinusoidal curve. In case “E”, it is experimentally observed that the voltage waveform seriously deviates from a sinusoidal curve .

In a previous work using a multiharmonic active load-pull and circuit simulation, much more square waveforms were reported [3]. However, in our experiment, the reflection coefficients of harmonics were not tuned intentionally. Table 2 shows that except for the fundamental frequency, these coefficients are almost the same. Differences in the waveforms between “G” and “E” are caused by a_1 for each harmonics generated in the HBT. Fig. 4 and Fig. 5 show the harmonics of i_c and v_c respectively when P_{out} is 30.5 dBm. In “E”, all harmonics except the third increases compared to “G”.

Fig. 6 and Fig. 7 show the dynamic load lines for “G” and “E”, respectively. In “G”, the harmonics are relatively small, therefore the trajectories are rather oval. In “E”, the trajectory at P_{out} of 30.5 dBm is quite distorted, reflecting the square-like waveform.

The previous paper[4] reported that the load line under efficiency matched operation should be inclined toward the horizontal position than under the gain matched operation. In our experiment, the load impedance for the fundamental frequency is 5.7Ω–j2.2Ω in “E” and 4.8Ω–j4.8Ω in “G”. This result is consistent with the reported one.

For power transistors, safety operating area should be carefully considered, especially for bipolar devices. Dynamic load line clearly shows operating area of a transistor. As shown, even for a 3.5V-operation, v_c exceeds 8 V in a moment. The device breakdown voltage should be three times greater than the operation voltage.

Conclusion

We showed experimentally measured dynamic load lines of the HBT when tuned to maximum collector efficiency and maximum gain. The trajectory of the dynamic load line is non-oval at the output power where the gain compression heavily occurs. This happens to transistors in high efficient operation because the output waveform is square-like than sinusoidal. In the case of efficiency-matched operation, all harmonics except the third grow compared with gain-matched operation, and it was confirmed that the instantaneous collector voltage reaches its lowest level when the instantaneous collector current reaches its maximum.

Acknowledgment

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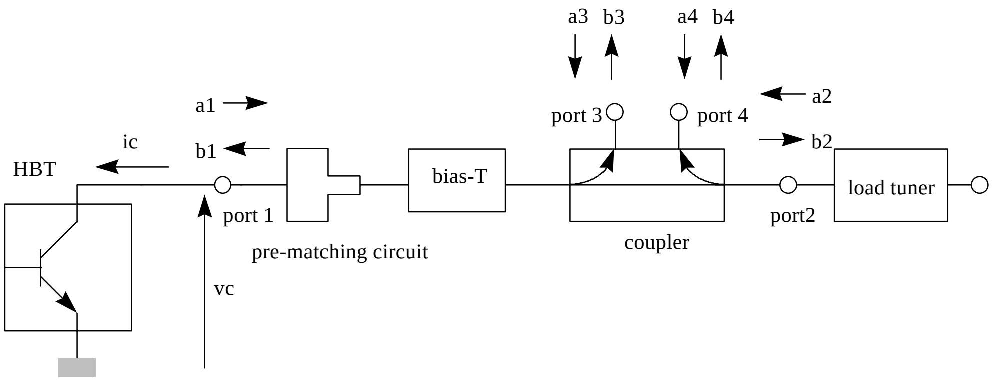

Fig. 1. Schematic of setup for the dynamic load line measurement.

Table 1. Summary of measured data.

Case	Pout (dBm)	Gain (dB)	Gain compression (dB)	Collector efficiency (%)	Collector DC current (A)	Collector DC voltage (V)
"G"	30.5	12.5	1.0	54.9	0.576	3.50
"G"	27.1	13.3	0.2	35.9	0.397	3.50
"G"	24.1	13.4	0.1	24.0	0.300	3.50
"E"	30.6	9.6	4.7	64.7	0.489	3.50
"E"	27.0	13.8	0.5	43.4	0.321	3.50
"E"	24.1	14.1	0.2	27.7	0.258	3.50

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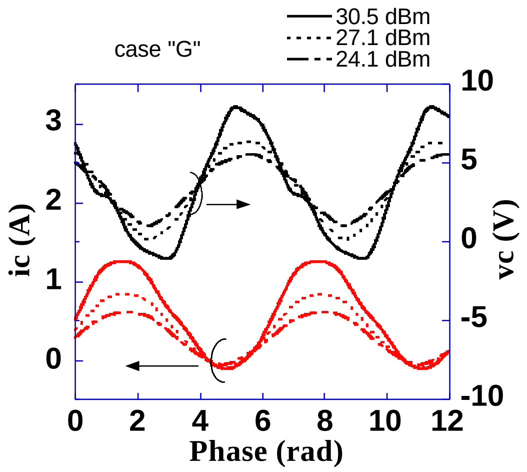

Fig. 2. Instantaneous collector current and voltage waveform measured with load tuned to maximum gain.

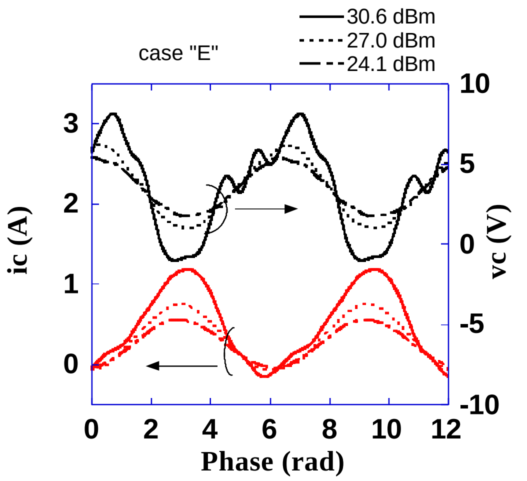

Fig. 3. Instantaneous collector current and voltage waveform measured with load tuned to maximum η_c.

Table 2. Reflection coefficient.

Harmonics	Case "G"	Case "E"
Fundamental	0.825 < -169	0.795 < -175
2nd	0.938 < 150	0.925 < 152
3rd	0.825 < 119	0.833 < 118
4th	0.899 < 170	0.898 < 170
5th	0.917 < 116	0.919 < 116

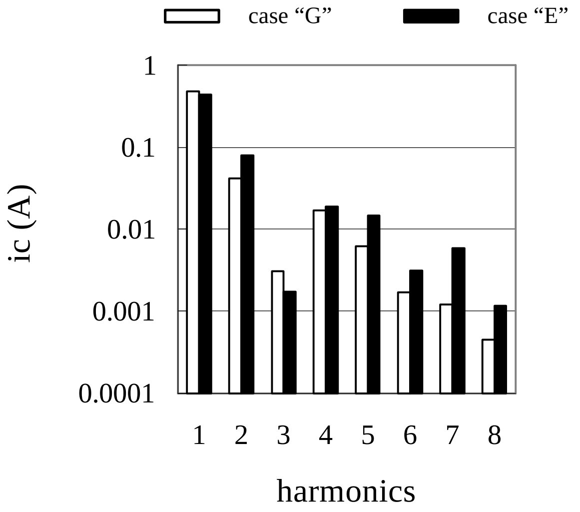

Fig. 4. Harmonics of i_c when P_{out} is 30.5dBm.

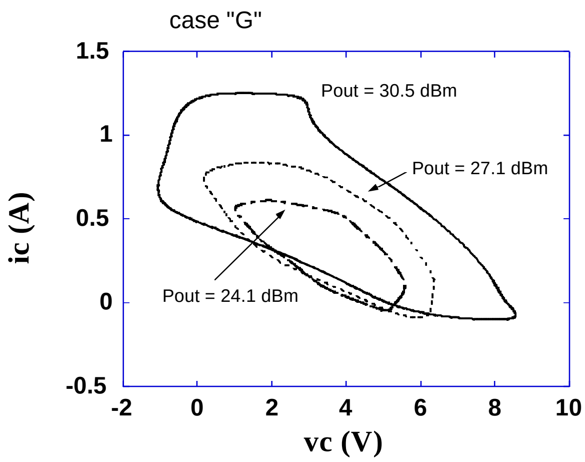

Fig. 6. Dynamic load lines with load tuned to maximum gain.

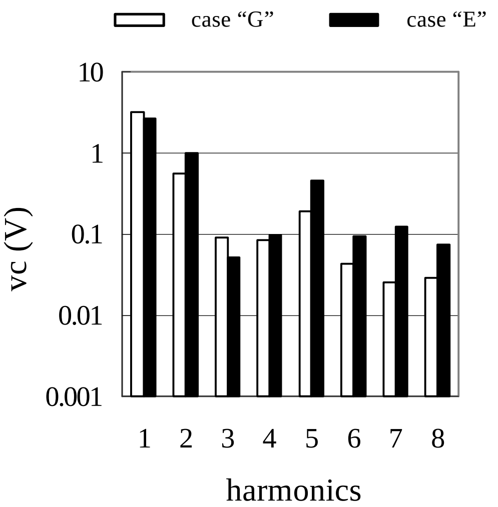

Fig. 5. Harmonics of v_c when P_{out} is 30.5dBm.

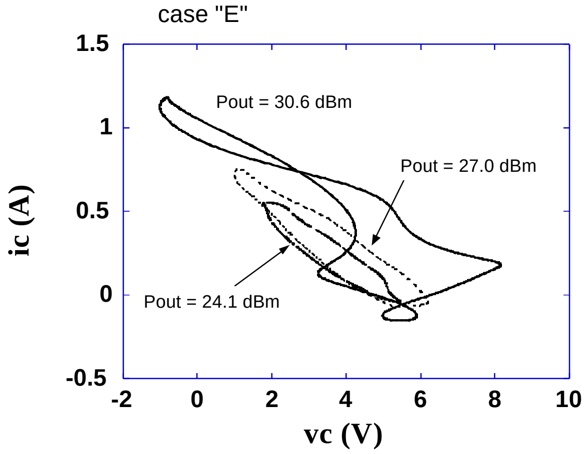

Fig. 7. Dynamic load lines with load tuned to maximum η_c.